REMARKS

By this Amendment, Applicants have amended claims 1, 4-7, and 9-12, and have cancelled claims 2, 3, and 8. Accordingly, claims 1, 4-7, and 9-14 are pending.

DRAWING OBJECTION

Figure 1 is objected to for reasons set forth in numbered paragraph two of the Office Action. To overcome this objection, Applicants are concurrently filing a Requests for Approval of Drawing Correction whereby Applicants overcome the objection by adding the legend "Prior Art". No new matter is added by this drawing change. As amended, Figure 1 is consistent with its description in Applicants' specification. Applicants therefore request that the objection to Figure 1 be withdrawn.

OBJECTION TO THE SPECIFICATION

The specification is objected to for reasons set forth in numbered paragraph three of the Office Action. Applicants have amended the specification at page 3, to overcome the basis for this objection.

In addition, the specification is objected to because of the number "M" at page 9, lines 24-30. Specifically, the Office Action states that number "M" is "not defined explicitly". Applicants respectfully disagree. Applicants point to the statements found at page 9, lines 27-29 and contend that one skilled in the art reading this description of the number "M", as well as the numerous references to the number "M" throughout the specification will readily understand the definition of the number "M".

Based on the foregoing, Applicants request that the objections to the specification be withdrawn.

CLAIM OBJECTIONS

Claims 2 and 7 are objected to for reasons set forth in number paragraph 4 of the Office Action. Applicants have cancelled claim 2 and have amended claim 7 to overcome the basis for the claim objection.

CLAIM REJECTIONS UNDER SECTION 112

Claims 5 and 6 stand rejected under 35 U.S.C. Section 112, second paragraph, for reasons set forth in numbered paragraphs 6 and 7 of the Office Action. Following the guidance of the Examiner, Applicants have amended claims 5 and 6 to more clearly define Applicants' claimed invention. Applicants submit that as result of these amendments to claims 5 and 6, the Section 112 rejection should be withdrawn. Applicants also contend that all claims are in full compliance with Section 112.

CLAIM REJECTIONS UNDER SECTION 103

Claims 1-6 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' admitted prior art ("APA") in view of Kamei. Applicants respectfully traverse this Section 103(a) rejection.

Claim 1 is an independent claim to which claims 4-6, 12, 13 and 14 either directly or indirectly depend. Claim 1 is directed to a light-emitting thyristor matrix array formed on a chip. Applicants have amended claim 1 to more clearly define Applicants' claimed invention. One of the features of amended claim 1 is as follows:

> the number M of the gate-selecting lines is selected so as to satisfy the expression of $L/\{(N/M)+M\} > p$ (L is a length of the long side of the chip and p is a critical value of the array pitch of bonding pads) in order to decrease the area of the chip.

This feature of the light-emitting thyristor matrix array of claim 1 is hereinafter generally referred to as the "Decreased Chip Area Feature" of Applicants' claimed invention. It is Applicants' position that none of the references of recorded either teach or suggest the Decreased Chip Area Feature and thereby Applicants' claimed invention is patentably distinguished from all of the references of record. There are, however, other features of Applicants' claimed invention which are not taught or suggested in any of the references of record, which will be subsequently explained.

An advantage of the light-emitting thyristor matrix array of Applicants' claimed invention is that the area of a chip on which the light-emitting element matrix array is formed can be decreased. To decrease the area of the chip, {(N/M)+M} bonding pads are arrayed in one line parallel to a long side of the chip to make the length of a short side of the chip small. The bonding pads are arrayed in one line by increasing the number M of a gate, anode or cathode-selecting lines to decrease the number of bonding pads. Thus, the number M of the selecting lines is selected so as to satisfy the expression of $L/\{(N/M)+M\} > p$. In other words, Applicants' claimed invention incorporates the Decreased Chip Area Feature which is not found in any of the references of record.

The APA concerns a light-emitting thyristor matrix array shown in Figure 1 of the subject application and discussed generally as pages 2-4. But the APA does not teach or suggest the Decreased Chip Area Feature of Applicants' claimed invention. The Decreased Chip Area Feature is also lacking in the Kamie Reference. Nowhere in the Kamie Reference is there any teaching or suggestion of this Feature.

Applicants have amended claim 1 by deleting the reference to "a plurality of bonding pads arrayed in one line in parallel with the long side of the chip". The Office Action admits that this feature is not taught in the APA, but takes the position that the Kamie Reference discloses a plurality of bonding pads arrayed in one line in parallel with the long side of "the chip". And in this connection, the Office Action points to bonding pads 9a in Figures 1 and 2 of the Kamei Reference. But even though the above quoted language has been deleted from claim 1, "the chip" is nonetheless not shown in Figures 1 and 2 of the Kamie Reference.

Figures 1 and 2 of the Kamie Reference show bonding pads 9a-9d provided on each resistor body 8, light-emitting elements 5 and contact electrodes 7 provided on a semiconductor body 4, and selected bonding pads 9a-9d and contact electrode 7 are connected by a bonding wire 10. A light-emitting element array 3 includes the semiconductor body 4, and the light-emitting elements 5 and contact electrodes 7 are provided thereon. Based on the foregoing description, the light-emitting element array 3 itself is a chip. Thus the bonding pads 9a-9d are not provided on a chip. Accordingly the Office Action is mistaken as to the Kamie Reference teaching a plurality of bonding pads on the chip.

Applicants' amended claim 1 also includes the feature of {(N/M)+M} bonding pads arrayed in one line in parallel with the long side of the chip (hereinafter referred to as the "Bonding Pad Feature" of Applicants' claimed invention). This Feature concerning bonding pads arrayed on the chip is not taught or suggested in the Kamie Reference. Thus this is an additional Feature patentably distinguishing Applicants' claimed invention from the Kamie Reference.

Applicants further note that the purpose of the Kamie Reference is to facilitate adjusting the light amount through selected bonding pads 9a, 9b, 9c or 9d for each light-emitting element 5, so that the brightness of the light of the light-emitting elements becomes equal when they are driven by the same voltage. This purpose or objective of the Kamie Reference has no relation or bearing relative to the objective or purpose of Applicants' claimed invention to decrease the area of the chip itself. Thus it is not surprising that the Kamie Reference does not teach or suggest the above noted Features of Applicants' claimed invention.

Based on the foregoing remarks, Applicants respectfully submit that claim 1 and dependent claims 1, 4-6, 12, 13 and 14 are patentably distinguished form the APA and the Kamie Reference. Accordingly, the Section 103(a) rejection based on these references should be withdrawn.

Claims 7-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the APA and Kamie in view of Breeze. Applicants respectively traverse this Section 103(a) rejection.

Claim 7 has been amended as an independent claim and as amended includes the Decreased Chip Area Feature and Bonding Pad Feature. On the basis of these Features, claim 7 and dependent claims 9-11 are neither taught nor suggested by the APA and the Kamie Reference. It is Applicant's contention that the Breeze Patent does not rectify these deficiencies of the APA and the Kamie Reference.

The Breeze Patent relates to a bi-directional drive multiplexed display system for use with multicharacter displays. In the Breeze system, each character is composed of a plurality of segments which are of a unidirectional type. Selected segments of each character are sequentially illuminated to display alphanumeric or other

symbols. In the Breeze system, the number of interconnections between the display and the drive circuit are reduced. The Breeze Patent was primarily cited with respected to light-emitting diode arrays. But nowhere in the Breeze Patent is there any teaching or suggestion of the Decreased Chip Area Feature and the Bonding Pad Feature of Applicants' claimed invention. Thus the combination of the APA, Kamie Reference and Breeze Patent does not teach or suggest the light-emitting thyristor matrix array formed on a chip as defined in Applicants' claim 7. Therefore, Applicants request that the Section 103(a) rejection based on these references be withdrawn.

Claims 13-14 stand rejected under 35 U.S.C. Section 103(a) as being unpatentable over APA and Kamie in view of Mead. Applicants respectively traverse this Section 103(a) rejection.

Claims 13 and 14 are ultimately dependent on claim 1 and therefore include the Decreased Chip Area Feature and the Bonding Pad Feature. These Features are not taught in the APA and Kamie Reference as discussed above. It is Applicant's position that the deficiencies of these references are not overcome by the Mead Patent.

The Mead Patent in general relates to an integrating imaging system with a phototransistor. The Mead Patent has been cited primarily with respect to parallel or serial input/output registers. But there is simply no teaching or suggestion in the Mead Patent of the Decreased Chip Area Feature and the Bonding Pad Feature of Applicants' claimed invention. Thus the combination of these references does not teach or suggest Applicants' invention as set forth in dependent claims 13 and 14. Applicants therefore request that the Section 103(a) rejection directed to claims 13 and 14 be withdrawn.

In view of the foregoing remarks and amendments, Applicants respectfully submit that claims 1, 4-7 and 9-14 are condition for allowance. Reconsideration and allowance of all pending claims are respectfully requested.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

SPECIFICATION:

Specification at page 3, lines 8-21:

Using the light-emitting thyristor matrix array, the number of bonding pads on a matrix array chip may be decreased. The number M of the gate-selecting lines in this structure in which the number of bonding pads may be decreased is selected in such a manner that M is an integer near to $N^{1/2}$ and N/M is an integer. For example, when M=8 or M=16 is selected in case of N=128, the number of bonding pads is 24 and this is minimum value. Therefore, it is possible to make the chip area small, resulting in the decrease of the chip cost. The circuit structure in Fig. 1 using light-emitting thyristors has been proposed by the present applicant, and Japanese Patent has already been issued (Japanese Patent No. 2807910) ~~that is incorporated herein by reference~~.

CLAIMS:

1. (Amended) A light-emitting thyristor matrix array formed on a chip, comprising:

N (N is an integer $\geqq$ 2) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip; ~~and~~

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected;

M (M is an integer $\geqq$ 2) gate selecting lines; and

{(N/M) + M} bonding pads arrayed in one line in parallel with the long side of the chip,

wherein the gate of kth light-emitting thyristor is connected to ith [i ={(k-1) MOD M} +1] gate-electing ling G_i, where "MOD" in an equation means modulo division,

the anode or cathode which is not connected to the common terminal of the kth light-emitting thyristor is connected to jth [$j = \{(k-i)/M\} + 1$] anode terminal A_j or cathode terminal K_j, and

the number M of the gate-selecting lines is selected so as to satisfy the expression of $L/\{(N/M) + M\} > p$ (L is a length of the long side of the chip and p is a critical value of the array pitch of the bonding pads) in order to decrease the area of the chip

~~a plurality of bonding pads arrayed in one line in parallel with the long side of the chip~~.

Claim 2 has been deleted.

Claim 3 has been deleted.

4. (Amended) The light-emitting thyristor matrix array of claim ~~3~~1, wherein the critical value p of the array pitch of the bonding pads is about 75 μm.

5. (Amended) The light-emitting thyristor matrix array of claim ~~3~~1, wherein when a prime factor for N is 2 only, the number M of the gate-selecting lines is positive and is the smallest integer, next smaller integer, or third smaller integer that satisfies the expression $L/\{(N/M) + M\} > p$.

6. (Amended) The light-emitting thyristor matrix array of claim ~~3~~1, wherein when prime factors for N are 2 and 3 only, the number M of the gate-selecting lines is positive and is the smallest integer, next smaller integer, third smaller integer, fourth smaller integer, or fifth smaller integer that satisfies the expression $L/\{(N/M) + M\} > p$.

7. (Amended) ~~The~~ A light-emitting thyristor matrix array ~~of claim 1, further~~formed on a chip, comprising:

N (N is an integer $\geqq$ 2) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip;

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected; ~~and~~

M (M is an integer ≧2) anode-selecting lines or cathode-selecting lines; and

{(N/M)+M} bonding pads arrayed in one line in parallel with the long side of the chip,

wherein the anode or cathode of kth light-emitting thyristor is connected to ith [i={(k-1) MOD M} + 1] anode-selecting line A_i or cathode-selecting line K_i, where "MOD" in an equation means modulo division,

the gate of the kth light-emitting thyristor is connected to jth [j={(k-i)/M} + 1] gate terminal G_j and

the number M of the anode-selecting lines or cathode-selecting lines is selected to satisfy the expression $L/\{(N/M)+M\}>p$ (L is a length of the long side of the chip and p is a critical value of array pitch of the bonding pads) in order to decrease the area of the chip.

Claim 8 has been canceled.

9. (Amended) The light-emitting thyristor matrix array of claim 87, wherein the critical value p of the array pitch of the bonding pads is about 75 μm.

10. (Amended) The light-emitting thyristor matrix array of claim 87, wherein when a prime factor for N is 2 only, ~~the number~~ M ~~of the anode-selecting lines or cathode-selecting lines is~~ is positive and is the smallest integer, next smaller integer, or third smaller integer that satisfies the expression $L/\{(N/M)+M\}>p$.

11. (Amended) The light-emitting thyristor matrix array of claim 87, wherein when prime factors for N are 2 and 3 only, ~~the number~~ M ~~of the anode-selecting lines or cathode selecting lines is~~is positive and is the smallest integer, next smaller integer, third smaller integer, fourth smaller integer, or fifth smaller integer that satisfies the expression $L/\{(N/M)+M\}>p$.

12. (Amended) A driver circuit for driving the light-emitting thyristor matrix array according to any one of claims ~~2-6~~1, 4, 5, and 6, comprising:

a circuit for driving the gate-selecting lines; and

a circuit for driving the anode terminals or cathodes terminal;

wherein the circuit for driving the gate-selecting lines including an even number of gate-selecting signal output terminals and a circuit for outputting a "selecting" signal to one of the gate-selecting signal output terminals and "no-selecting" signal to the others of the gate-selecting signal output terminals, with the terminal to which the "selecting" signal is supplied being switched in turn.